Eng. Research Bull.
Faculty of Eng. & Tech.,
Menoufia University.
Vol. VII Part II, 1985.

PP. 251-257

DESIGN AND REALISATION OF A SIMPLE I.C's TESTER.

Hossam H. Ahmed Abdel-Al. O. Attia.

Eac. of Electronic Eng., Menoufia, Univ., Egypt.

ABSTRACT:

One of the most important steps in any maintenance of an electronic circuit, is the electronic component performance indication.
Nowadays, I.C's are the most pupular used components. This makes the I.C's testing very essential for starting any electronic circuit checking up or construacting up.

In this work, it is aimed to design an I.C's tester followed by its construction and its utilization to test various I.C's .

A very simple circuit consists of V.R. power supply, function generator, counter and display has been designed using I.C's sockets (plug-in). The design is orinted for testing the most popular I.C's, i.e 555, 741, CA 3130, TL 081, LM 324, 4001, 4011, 4017, 4027, 7400, 7402, 7490 and the 7-segment common cathod.

The designed and contructed circuit indicate very simple and satisfactory testing tool for the mentioned I.C's. It can be modified for various I.C's testing.

INTRODUCTION :

It is essential to test the I.C's in a quite manner just to indicate its validity for utilization. For maintentance purposes, it is also important to start with

such testing to detect and locate the fault. Many authers designed and construct various testers considering specified parameters for specified application.

However for general applications and maintenance requirements, general tester is essentially required. In this work, a general tester has been designed, constracted and the most popular used I.C's have been tested.

I.C'S TESTER DESIGN AND CONSTRUCTION:

The testing scheme depends on generating an input specified signal and check the output by using signal detection device, i.e. light emitting diode (LED). This simplify the required circuit to be composed of : voltage regulated power supply, function generator, as illustrate in Fig. (1).

A- FUNCTION GENERATOR :

This has been designed using LM555 and DC-voltage = 9 v. The chosed resistance and capacitor give square pulses of 5 Hz frequency. The LM555 is followed by JK-flip-flop 4027 to give clock pulses of 2.5 Hz frequency with two output amplitude i.e 5 v for the TTL I.C's, and 9 v for the C-MOS-I.C's. Follower emitter transistors has been added Q_1, Q_2, to give protection against the reflected signales. The zener diode Z_1 (5 v) is added to be considered as refrence voltage. Further protective elements for Q_1 , Q_2 as R_7, R_{10} and R_{27} against any fault.

Two LED have been used so as one of them give its light at 5 V (S5), while the second give its light at 9 v (S9). They are used as indicated elements.

B- LOGICAL GATES :

The inputs of NAND or NOR gate are connected in series, then the gat is work as inverter. CMOS 4001 or 4011 have four gates i.e even numbers and the four inverters give an output in phase with the input as shown in Fig. (2) .

The voltage supply to the TTL circuits is regulated by a small voltage regulator 78LO5 which reduced 9 to 5 volts.

C- THE OPERATIONAL AMPLIFIERS :

The operational amplifiers 741 has been selected and used in the non-inverting mode, and the op. Amp. CA3130 has been also selected. Both of them has been connected as in Fig. (2). The R_f is cancelled, when the op. Amp. 741 and LM324 are used, which give unit voltage gain i.e $V_o = V_i$.

But for CA3130, R_i, R_f have been used i.e R_{23}, R_{22} respectively as in Fig. (3). R_{23} has been choosen to be 47 K Ω and R_{22} has been estimated to give a net voltage gain = 2.45

$\therefore R_{22} = 68$ K Ω, $R_{24} = 1$ K Ω

The whole circuit is shown in Fig. (2).

D- THE COUNTERS :

i) Using TTL :

This has been designed so as to divide the output frequency (i.e 2.5 Hz) by 10 as shown in Fig. (4). LED has been added to indicate the output which is protected by $R_{25} = 270$ Ω .

ii) Using C-Mos -4017 :

The used circuit is very simple and works by its input No. 14 with +ve pulse with frequency 2.5 Hz. This is given by S9 Fig. (1). This give a +ve pulse every 0.4 sec.

The ten outputs of 4017 are connected to the 7-segment display and two LED's [D_3, D_4 Fig. (4)] .

The currents through D_3, D_4 have been limitted by R_{11} Fig. (4). R_{11} has been calculated as :

The output voltage of C-Mos I.C's
8.2 V as the clock voltage = 9 V

$\therefore R_{11} = (8.2 / 11 \text{ m.A}) \cong 820\ \Omega$

10 m.A is the total current for D_3, D_4 [1, 2].
The complete circuit is shown in Fig. (4).

The final designed circuit has been layed out and constructed, as shown in Fig. (5).

EXPERIMENTAL WORK :

The constructed circuit has been used for testing the following standard and widely used I.C's.

1- OP-AMP. 741 :

About 10 pieces have been tested very simply as it has been indicated through the LED that when it emitts light, the I.C's is all-wright and if no emission it is not. The results indicate that 7 of them are good while 3 of them are not. This agreed with the expected results.

2- LM555 :

23 pieces have been tested 17-pieces are good and 6 pieces are not.

3- NAND, AND, OR, NOR LOGICAL GATES :

Huge number of such gates have been tested and the indicated results agreed with the expected results.

CONCLUSION :

The proposed, designed and constructed circuit give satisfactory tests for the standard I.C's. Also other I.C's encluding the microwave I.C's can be tested by using microwave signals.

This circuit can be scaled up to give more utilisation.

REFERANCES :

1. National Semiconductor Data-Sheet (1982).
2. The TTL Data Book, Vol. 1 (1983/84) texas instruments.
3. Albert Paul Malvino, Digital Computer Electronics, McGraw-Hill, Reprinted (1982) .
4. Thomas C. Bartee, Digital Computer Fundamental Fifth Edition. (1982).
5. Albert Paul Malvino, Electronic Instrumentation Fundamentals, McGraw-Hill (1967).
6. Morton H. Lewin, Logic Design and Computer Organization, McGraw-Hill (1981).

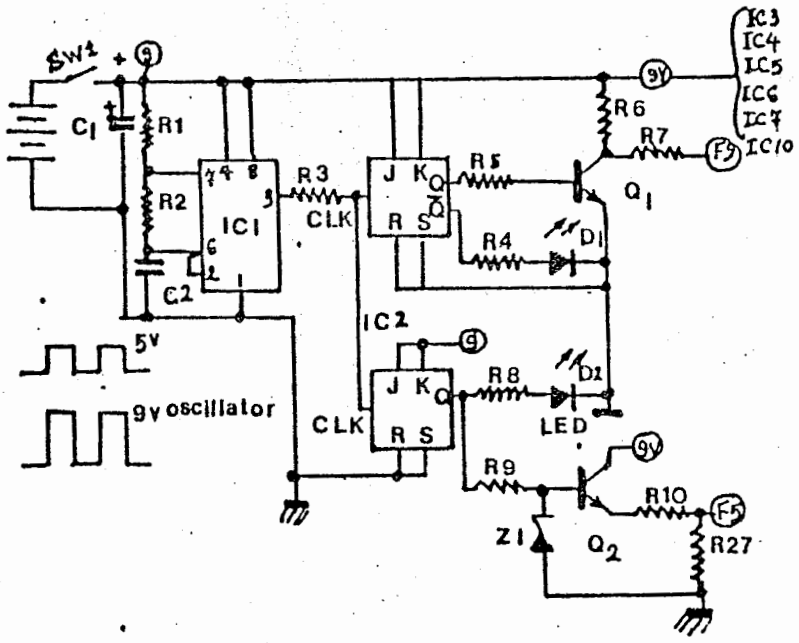

SW1
9
C1
R1
R2
C2
IC1
R3
CLK
J K Q
R S
R5
R4
D1
Q1
R6
R7
9V
F5
IC3
IC4
IC5
IC6
IC7
IC10
IC2
5V
9v oscillator
R8
LED
R9
R10
R27
Z1
Q2

Fig.(1)

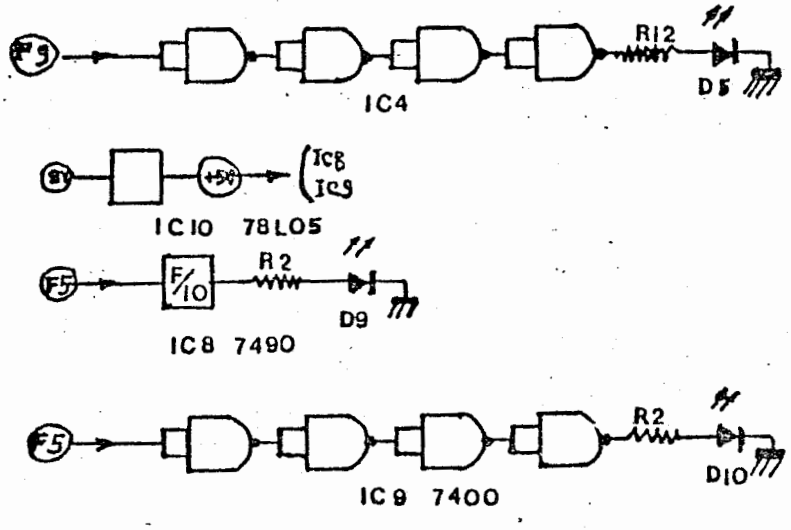
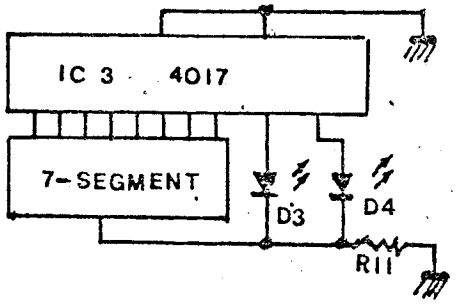

F9
IC4
R12
D5
IC10 78L05
R2
D9
IC8 7490
IC9 7400
D10

Fig.(2)



Fig(2)

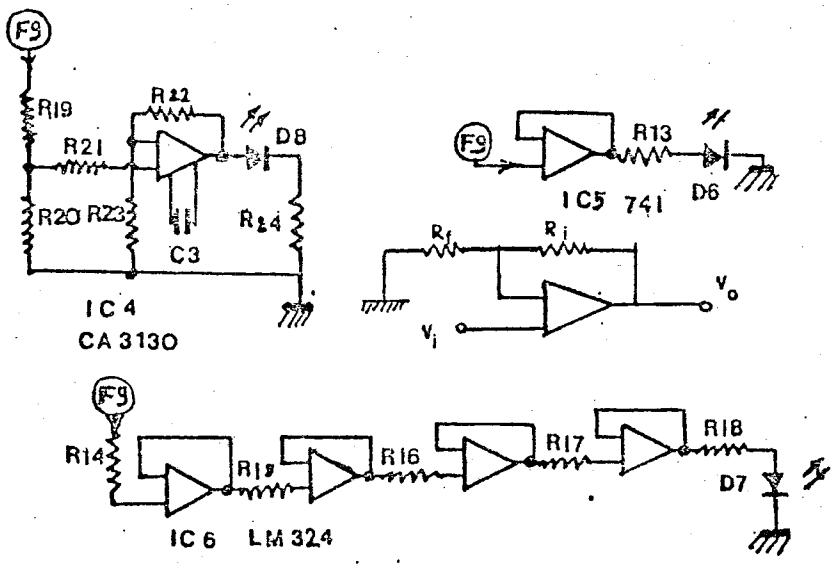


Fig.(3)

Fig(5)