Menoufia University
Faculty of Electronic Eng.
3rd year, CSE Dept.
CSE217
Elective Course IV.

Midterm exam (2nd Term)
Time: 60 min
Full mark = 20
Date: 3/4/2019
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الاسم:---------- الفصل:----------

Answer the following questions:

First question:.....(4 Marks)

(a) What are the three steps in VHDL to construct a circuit in a programmable device?

(b) Convert the following combinational equations into PLA-based circuit;
Use single PLA chip.
(PLA consists of programmable ANDs followed by programmable ORs).

F1 = a'.b + a

F2 = a.b' + a'

F3 = a ⊕ b

Draw your circuit design here →

Second question:.....(10 Marks)

Use the following TYPE definitions and SIGNAL declarations to solve (a) & (b):

```
TYPE row IS ARRAY (7 DOWNTO 0) OF STD_LOGIC;
TYPE array1 IS ARRAY (0 TO 3) OF row;
TYPE array2 IS ARRAY (0 TO 3) OF STD_LOGIC_VECTOR(7 DOWNTO 0);
TYPE array3 IS ARRAY (0 TO 3, 7 DOWNTO 0) OF STD_LOGIC;
```

---------Beside each SIGNAL write its dimensionality---------

```
SIGNAL x: row; --_____
SIGNAL y: array1;--_____
SIGNAL v: array2;--_____
SIGNAL w: array3;--_____
SIGNAL a : BIT := '1';--_____
SIGNAL b : BIT_VECTOR (3 DOWNTO 0) := "1100";--_____
SIGNAL c : BIT_VECTOR (3 DOWNTO 0) := "0010";--_____
SIGNAL d : BIT_VECTOR (7 DOWNTO 0);--_____
SIGNAL e : INTEGER RANGE 0 TO 255;--_____
SIGNAL f : INTEGER RANGE -128 TO 127;--_____
```

(a) Determine legal and illegal statements :

```
x(0) <= y(1)(2); --_____
x(2) <= w(2)(1); --_____
w(3,0) <= v(0)(3); --_____
x <= v(1);--_____
y(1)(7 DOWNTO 3) <= x(4 DOWNTO 0);--_____
if(e>d) --_____
b sra 1 --_____
f sll -1 --_____
```

(b) Fill the following blanks:

```
x1 <= b XOR c; -> x1 <= _____
x2 <= b sll 2; -> x2 <= _____
x3 <= b sla 2; -> x3 <= _____
d <= (5=>'0', OTHERS=>'1'); -> d<= _____
d'HIGH -> _____
c'LEFT -> _____
d'LENGTH -> _____
b'RANGE -> _____
```

Third question:.....(6 Marks)

(a) Write VHDL code to implement the circuit in fig.1.

(b) Write VHDL code to implement Generic Parity Detector (fig.2). The circuit must provide Output '0' when the number of '1's in the input vector is even, OR output '1' otherwise.

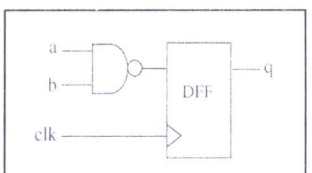

Fig1

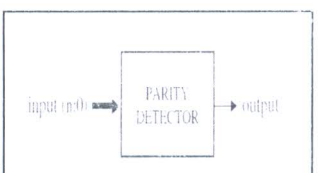

Fig2

With my best wishes *(Use the back of the paper)*