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University

Menoufia

Faculty

Electronic Engineering

Department

Communication and

Networking Eng.

Academic level:

Course Name **Digital Electronics**

Course Code **ECE 375**

Date

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Full Mark Exam

40 Marks **Final Exam**

Examiner

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Answer the following Questions

Question 1

(10M)

a) Design a 4 bit shift register. Give an illustrative example, if the initial value is 0010 and there is 5

clocks and the input changes from 1 to 0 after clock 2.

(2M)

b) What is the difference between 3bit ripple counter and 3bit synchronous counter?

(2M)

c) Design a Mod-5 synchronous counter using J-K Flip-Flops.

(6M)

Question 2

(6M)

As an electronic engineer, you have given the following Boolean function (F)

$$F(W, X, Y, Z) = \sum_{i} m(1, 3, 4, 11, 12, 13, 14, 15)$$

- i) implement F by using 4×1 MUX and external gates, when the inputs W and X are only used as selection lines?
- ii) implement F by using two 8×1 MUX
- iii) implement F by decoder

Question 3

(9M)

a) What is the types of PLDs. State the advantages of PLDs and what the difference between PROM,

PAL and PLA?

(3M)

b) Design a full adder by the following IC PLDs

(6M)

i) PROM

ii) PAL

iii) PLA

Question 4

(15M)

a) Describe the major types of sequential PLDs. Use figures to explain your answer. (3M)

b) Define look up table (LUT). Suppose we want to realize a Boolean Function of four input variables A, B, C and D using FPGA with 4-input LUT. Let the output is high only when any of the two input variables are 1. Give illustrative example for the output when the inputs is 0111. What do we do when our FPGA does not have a 4-input LUT, but only 3-input LUTs? Can we implement (7M)our function in it? How?

c) Write a VHDL Programming Code for the following function

(5M)

$$F = (A \oplus BC) + (\overline{A + C})$$

Draw the digital electronic circuit and time diagram.

Best wishes

Dr. Saied M. Abd El-atty