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A Modified Single-Stage Three-Phase Boost Inverter for PV Applications

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ABSTRACT
This paper proposes a single-stage three-phase boost inverter for Photovoltaic (PV) applications. The proposed circuit topology is directly step-up the input low level DC voltage to a high-level output AC voltage in only one stage, using an inductor and six switches. A new control methodology is introduced to regulate the AC output voltage and current and is suitable for grid-connected and stand-alone applications. The proposed circuit uses only six switches of a simple type of switches that achieve the desired objectives easily without additional antiparallel diodes. The circuit topology is extensively analysed and the overall performance including total harmonic distortion (THD) is obtained by computer simulation and presented under different conditions. A DSP-based laboratory model is built to assess the proposed single-stage three-phase boost inverter when fed from a PV source. The experimental results confirm the simulation, illustrating the successful operation of the proposed circuit topology to produce three-phase AC output from the low DC voltage of the PV source.

Keywords: *Renewable energy; Single-Stage converters; Boost Inverters; three-phase boost inverter*.

1. Introduction

Power conversion systems are extensively used today in different applications, such as uninterrupted power supplies (UPSs), induction heating, low-power drives and renewable energy (RE) sources. However, with the present emphasis on RE applications, more and more effort is required to develop new circuit topologies that facilitate and improve the utilization of this energy. Power conversion circuits are required to perform several important interface tasks between the RE sources and grids or load applications. The first task is to boost the DC input voltage into a required voltage level and invert the DC voltage to AC voltage with a fixed frequency and amplitude. The second task is to utilize the maximum available power of these RE sources. In addition, the harmonic produced by such an interface is injected in the network have to be minimized

Various techniques have been developed to find solutions to the above-mentioned technical challenges, and several power conversion circuit topologies have been presented in literature [1-18]. In Fig. 1(a), a step-up transformer is used after the inverter to boost the output voltage [1, 2]. This, however, has several disadvantages, such as loud noise, huge size, and high cost. Furthermore, the lower system efficiency as the transformer should be designed for a wide range of power, which leads to a low system efficiency. In Fig. 1(b), a two-stage circuit topology is used in which a DC-DC boost converter is used in cascade with the inverter [3]. The DC-DC converter boosts the output voltage of the RE sources and then the inverter converts the DC voltage to AC and to match the load requirements. Although these two stage topologies are simple, they suffer from low efficiency, less reliability, more losses, and high component count [4]. Moreover, the added DC-DC boost converter may increase inverter size and cost [5, 6]. This topology, in comparison with the topology displayed in Fig. 1(a), requires two individual control systems, one for the dc-dc converter and the other for the six switches inverter. This will result in a lower reliability and efficiency, as well as a more complicated control scheme [7]. Another option to interface these RE sources is the three-phase multilevel inverters that presented in [8]. Although these multilevel inverters are effective for RE sources, the additional components to the circuit reduce the overall efficiency and reliability of the system. Other topology has been presented as an interface is shown in Fig. 1(c) which is called the z-source inverter. The z-source inverter has the ability

of boosting and inverting the DC voltage in to AC voltage in only a single stage, with fewer switches in comparison with the aforementioned two-stage topology depicted in Fig. 1(b). This type of inverters has a fast evolution during the last few years in order to replace the conventional two-stage topology, since the first release of the three-phase Z-source inverter (ZSI) was in 2003 [9]. Recently, many research activities have been established in order to improve the ZSIs performance from different perspectives, such as high input current ripples, overall voltage gain, voltage stresses across different devices [10], continuity of the input current, and conversion efficiency, and high component count [11–16]. Among these different topological improvements, the three-phase quasi-ZSI and hybrid switched boost inverter (hybrid-SBI) in which the voltage stresses across dc-link inductors and capacitors is reduced [17, 18]. The quasi-ZSI consists of two capacitors, two inductors that are connected to six switches that increase the size, weight and cost of the power inverter. While the hybrid-SBI uses one less inductor and one more diode when compared with the three-phase quasi-ZSI.

This paper proposes a configuration topology for a high performance single stage three- phase boost inverter to avoid the above mentioned disadvantages using a reduced number of power electronic switches compared with those used in previous inverter topologies. The proposed circuit uses only six switches of a simple type of switches that achieve the desired objectives easily without additional antiparallel diodes which simplifies the circuit configuration. As a result, the proposed configuration offers the advantages of reducing complexity of control circuit and size compared with previous inverter topologies. A new control methodology is proposed that regulates the AC output voltage and current closely to a sinusoidal waveform. The principle of operation and control of the three-phase proposed inverter are presented. Detailed analysis and modelling of the proposed inverter is presented and the waveforms of voltage, current and their harmonics spectrum are discussed and verified in detail. The state equations which describe the modes of operations for the proposed topology are presented. Finally simulation and experimental results verifying the validity of the proposed analysis under different conditions are analyzed and discussed.

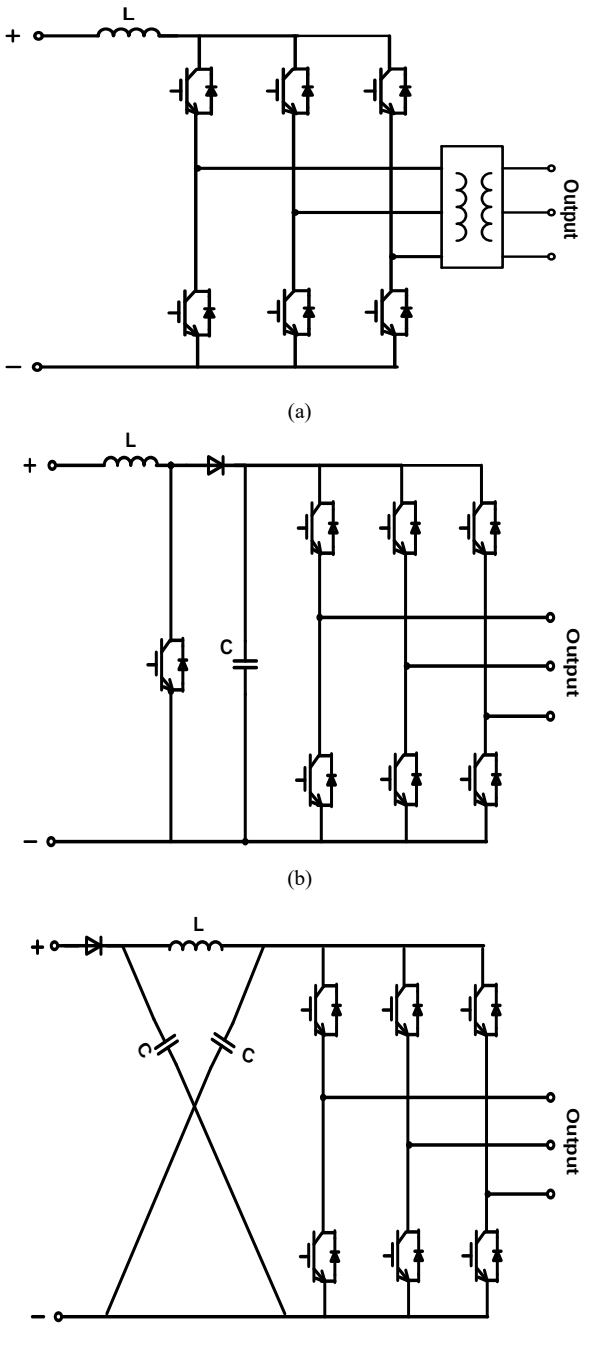


Fig.1. Connections of PV sources to utility grids and stand-alone

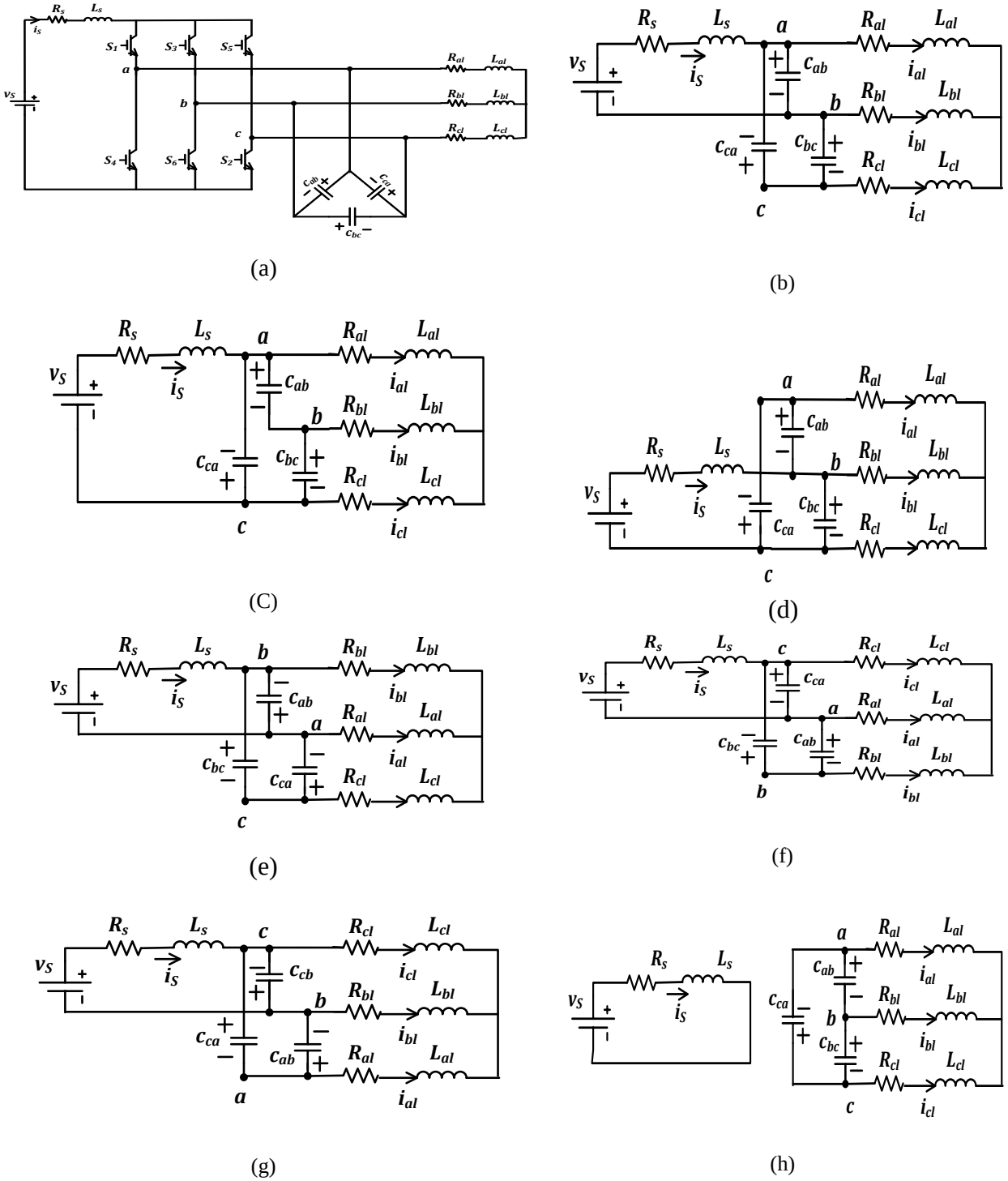


Fig. 2. Circuit diagrams for the proposed boost inverter and modes of operations:(a) The Proposed single-stage three-phase boost inverter,(b) Equivalent circuit during Mode 2,(c) Equivalent circuit during Mode 4,(d) Equivalent circuit during Mode 6,(e) Equivalent circuit during Mode 8,(f) Equivalent circuit during Mode 10 ,(g) Equivalent circuit during Mode 12 , (h) Equivalent circuit during Modes 1,3,5,7,9 and 11.

2. The Proposed Inverter Topology And Principle Of Operation

This section briefly describes the proposed topology. The proposed topology is a three-phase boost inverter with one single-stage. The developed switching pattern is formulated based upon new control strategy that will be explained in the next section. The power topology and switching pattern arrangement has been offered for the purpose of continuity. Fig. 2 shows the schematic diagram of the proposed inverter. The proposed inverter topology consists of only six switches (S1, S2, S3, S4, S5, and S6) arranged as shown in Fig. 2(a) to regulate the power delivered to the load, and the boost inductor are located between the DC source and the inverter, where $\boldsymbol{v_s}$ is the DC source, L_s and R_s are the boost inductor and its resistance. AC side delta connection capacitors C_{ab}, C_{bc}, and C_{ca} to be charged during discharge time intervals and supply the three phase RL load determine by $(R_{aL}, R_{bL}, R_{cL}, L_{aL}, L_{bL}, and\ L_{cL})$ during charging times intervals. Also, Fig. 2 shows the schematic diagrams of each mode of operation for each switching interval. There are six switching intervals (ab, ac, bc, ba, ca, and cb) to form three phase voltages. At any switching interval, one of the upper switches is kept on, and two of the lower switches are operated in a manner determined by the control strategy. There are two modes for each switching interval, namely charging and discharging. During the charging time intervals, the switches in a same leg are simultaneously on so that the magnetic energy in L_s is increased, while in discharging time intervals, the energy is injected to the load

A. (Switching interval (ab

Mode 1 (power switches S_1 and S_4 are closed):
During this mode, the inductor current increases storing energy in the inductor L_s and the load is supplied by the energy stored in the delta connection capacitor C_{ab}, C_{bc}, and C_{ca}. Fig. 2(h) shows the equivalent circuit during this mode. Equations could be written as (assuming ideal switches):

$$v_s = i_s R_s + L_s \frac{di_s}{dt} \quad (1)$$

$$v_{ab} = i_{al} R_{al} + L_{al} \frac{di_{al}}{dt} - i_{bl} R_{bl} - L_{bl} \frac{di_{bl}}{dt} \quad (2)$$

$$v_{bc} = i_{bl} R_{bl} + L_{bl} \frac{di_{bl}}{dt} - i_{cl} R_{cl} - L_{cl} \frac{di_{cl}}{dt} \quad (3)$$

$$v_{ca} = i_{cl} R_{cl} + L_{cl} \frac{di_{cl}}{dt} - i_{al} R_{al} - L_{al} \frac{di_{al}}{dt} \quad (4)$$

$$i_{al} + i_{bl} + i_{cl} = 0 \quad (5)$$

Mode 2 (power switches S_1 and S_6 are closed):

During this mode, the voltage across the inductor L_s is reversed and the energy in the inductor L_s is transferred to the load and capacitors C_{ab}, C_{bc}, and C_{ca}. Fig. 2(b) shows the equivalent circuit during this mode. Equation could be written as (assuming ideal switches):

$$v_s = i_s R_s + L_s \frac{di_s}{dt} + v_{ab} \quad (6)$$

$$v_{ab} = -v_{bc} - v_{ca} \quad (7)$$

Where,

$$v_{ab} = i_{al} R_{al} + L_{al} \frac{di_{al}}{dt} - i_{bl} R_{bl} - L_{bl} \frac{di_{bl}}{dt} \quad (8)$$

$$v_{bc} = i_{bl} R_{bl} + L_{bl} \frac{di_{bl}}{dt} - i_{cl} R_{cl} - L_{cl} \frac{di_{cl}}{dt} \quad (9)$$

$$v_{ca} = i_{cl} R_{cl} + L_{cl} \frac{di_{cl}}{dt} - i_{al} R_{al} - L_{al} \frac{di_{al}}{dt} \quad (10)$$

$$i_{al} + i_{bl} + i_{cl} = 0 \quad (11)$$

Where v_{ab} is the difference voltage between point (a) and point (b), v_{bc} is the diff. voltage between point (b) and point (c), v_{ca} is the diff. voltage between point (c) and point (a), i_{al}, i_{bl}, i_{cl} are the three phase load currents, and i_s is the supply current.

B. (Switching interval (ac

Mode 3 (power switches S1 and S4 are closed):
Similarly as in mode 1, the inductor current increases storing energy in the inductor L_s and the load is supplied by the energy stored in the delta connection capacitor C_{ab}, C_{bc}, and C_{ca}.This mode equations and figure are the same of mode 1.

Mode 4 (power switches S_1 and S_2 are closed):

The same sequence of mode 2 is done as the voltage across the inductor L_s is reversed and the energy in the inductor L_s is transferred to the load and capacitors C_{ab}, C_{bc}, and C_{ca}. Fig. 2(c) shows the equivalent circuit during this mode. Equations could be written as in mode 2 except equations (6), (7) and (10) that could be written as:

$$v_s = i_s R_s + L_s \frac{di_s}{dt} - v_{ac} \quad (12)$$

$$v_{ac} = -v_{ab} - v_{bc} \quad (13)$$

$$v_{ac} = i_{cl} R_{cl} + L_{cl} \frac{di_{cl}}{dt} - i_{al} R_{al} - L_{al} \frac{di_{al}}{dt} \quad (14)$$

C. (Switching interval (bc

Mode 5 (power switches S_3 and S_6 are closed): Similarly as in mode 1.
Mode 6 (power switches S_3 and S_2 are closed): The same sequence of mode 2 is done. Fig. 2(d) shows the equivalent circuit during this mode. Equations could be written as in mode 2 except equations (6) and (7) that could be written as:

$$v_s = i_s R_s + L_s \frac{di_s}{dt} + v_{bc} \quad (15)$$

$$v_{bc} = -v_{ab} - v_{ca} \quad (16)$$

D. (Switching interval (ba

Mode 7 (power switches S_3 and S_6 are closed): Similarly as in mode 1.

Mode 8 (power switches S_3 and S_4 are closed): The same sequence of mode 2 is done. Fig. 2(e) shows the equivalent circuit during this mode. Equations could be written as in mode 2 except equations (6), (7) and (8) that could be written as:

$$v_s = i_s R_s + L_s \frac{di_s}{dt} - v_{ba} \quad (17)$$

$$v_{ba} = v_{bc} + v_{ca} \quad (18)$$

$$v_{ba} = i_{al} R_{al} + L_{al} \frac{di_{al}}{dt} - i_{bl} R_{bl} - L_{bl} \frac{di_{bl}}{dt} \quad (19)$$

E. (Switching interval (ca

Mode 9 (power switches S_5 and S_2 are closed): Similarly as in mode 1.

Mode 10 (power switches S_5 and S_4 are closed): The same sequence of mode 2 is done. Fig. 2(f) shows the equivalent circuit during this mode. Equations could be written as in mode 2 except equations (6) and (7) that could be written as:

$$v_s = i_s R_s + L_s \frac{di_s}{dt} + v_{ca} \quad (20)$$

$$v_{ca} = -v_{ab} - v_{bc} \quad (21)$$

F. (Switching interval (cb

Mode 11 (power switches S_5 and S_2 are closed): Similarly as in mode 1.

Mode 12 (power switches S_5 and S_6 are closed): The same sequence of mode 2 is done. Fig. 2(g) shows the equivalent circuit during this mode. Equations could be written as in mode 2 except equations (6), (7) and (9) that could be written as:

$$v_s = i_s R_s + L_s \frac{di_s}{dt} + v_{cb} \quad (22)$$

$$v_{cb} = v_{ab} + v_{ca} \quad (23)$$

$$v_{cb} = i_{bl} R_{bl} + L_{bl} \frac{di_{bl}}{dt} - i_{cl} R_{cl} - L_{cl} \frac{di_{cl}}{dt} \quad (24)$$

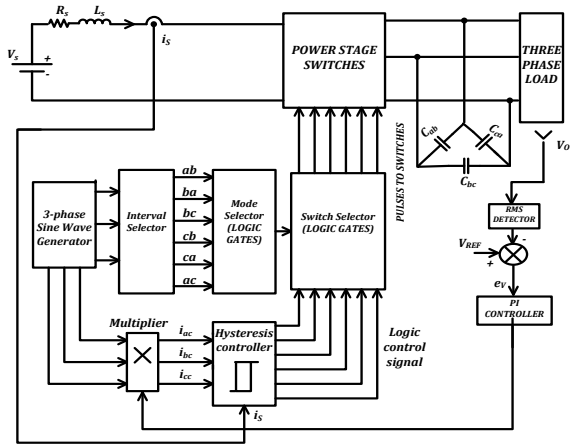
3. Proposed Control Strategy

The output waveform of the proposed three-phase inverter is required to be sinusoidal and of constant amplitude and frequency with minimum total harmonic distortion. So when designing a control circuit for these inverters, some of the characteristics that may be considered include sinusoidal output waveforms of voltage/current and fast transient responses for sudden changes are very important. cient fiThus, it is required to design a robust and ef control strategy especially that used in remote areas, renewable energy applications, and critical loads. Therefore, this section proposes a new control strategy which is utilized for the proposed boost inverter topology. The PWM switching pattern for the six switches will be developed and elaborated as follows:

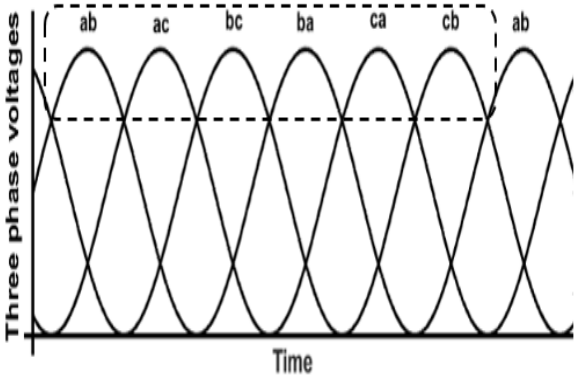
As the output circuit is a series R–L load, i.e., $z = r + j\omega l$, the line to-line phasor voltages are $v_{ab} = z\,(i_a - i_b)$, $v_{bc} = z\,(i_b - i_c)$, and $v_{ca} = z\,(i_c - i_a)$ in term of i_a, i_b, *and* i_c, which are the line currents of phases a, b, and c. The line-to-line voltages, v_{ab}, v_{bc}, and v_{ca}, waveforms become sinusoidal when the line current waveforms are sinusoidal. From this point, the proposed control depends on a new method of current control that control the switching pattern for each switch of the proposed inverter. This is done by making a control separation between the upper switches (S_1, S_3, S_5) and the lower switches (S_2, S_4, S_6). The upper switches are controlled by determining which one of the switching intervals needed to be controlled (*ab*, *ac*, *bc*, *ba*, *ca*, *cb*). This is done as shown in Fig. 3(a) where the 3-phase sine wave generator is passed through the interval selector block. The function of that block is to detect all the (*ab*, *ac*, *bc*, *ba*, *ca*, *and cb*) switching intervals. This step is done through a comparison between the three phase sine wave and detect the higher value for each phase as shown in Fig. 3(b). These switching intervals (*ab*, *ac*, *bc*, *ba*, *ca*, *and cb*) are become the input of the mode selector block. That is a logic AND& OR gates to separate each switching interval from the others, which are become the input to the switch selector block that it also a logic gates that control the six switches operations. One of the upper switches (S_1, S_3, S_5) is operated after determining which switching interval will be activated. On the other hand, two of the lower switches (S_2, S_4, S_6) are operated and controlled by the hysteresis controller block depending on which mode is activated under each switching interval. The process which the hysteresis controller depend on its operation is based on the current control operation. That is verified by the following, as the reference voltage signal (v_{ref}) is set according to the required load voltage, and by using a RMS value detector, the output load voltage is compared with that reference voltage signal (v_{ref}) and produce the error signal (e_v). This error signal (e_v) is passed through a proportional integral (PI) controller. The output of the controller is then multiplied by a three phase sine wave unit vector by the aid of 3-phase sine wave generator to produce the command currents (i_{ac}, i_{bc}, i_{cc})..The three phase command currents are compared with the supply current (i_s) through a hysteresis current controller to determine which mode is activated according to the operation modes as detailed in Table 1.

Table 1- Switching States for Each Operational Mode

INTERVAL	*ab*		*ac*		*Bc*		*ba*		*ca*		*cb*	
SWITCH	*Mode 1*	*Mode 2*	*Mode 3*	*Mode 4*	*Mode 5*	*Mode 6*	*Mode 7*	*Mode 8*	*Mode 9*	*Mode 10*	*Mode 11*	*Mode 12*
$_1S$	*ON*	*ON*	*ON*	*ON*	*OFF*	*OFF*	*OFF*	*OFF*	*OFF*	*OFF*	*OFF*	*OFF*
$_2S$	*OFF*	*OFF*	*OFF*	*ON*	*OFF*	*ON*	*OFF*	*OFF*	*ON*	*OFF*	*ON*	*OFF*
$_3S$	*OFF*	*OFF*	*OFF*	*OFF*	*ON*	*ON*	*ON*	*ON*	*OFF*	*OFF*	*OFF*	*OFF*
$_4S$	*ON*	*OFF*	*ON*	*OFF*	*OFF*	*OFF*	*OFF*	*ON*	*OFF*	*ON*	*OFF*	*OFF*
$_5S$	*OFF*	*OFF*	*OFF*	*OFF*	*OFF*	*OFF*	*OFF*	*OFF*	*ON*	*ON*	*ON*	*ON*
$_6S$	*OFF*	*ON*	*OFF*	*OFF*	*ON*	*OFF*	*ON*	*OFF*	*OFF*	*OFF*	*OFF*	*ON*



(a)



(b)

Fig. 3. Proposed control strategy.

4. Simulation Results

The proposed single-stage three-phase boost inverter with its control strategy has been built and simulated using MATLAB/SIMULNK software. Simulation is carried out to determine the characteristics of the proposed boost inverter. The circuit parameters of the prototype are listed in the Appendix A.

The steady state response of the proposed system is obtained as shown in Fig. 4. The dc supply is kept constant at 100 volt and the reference voltage is controlled to allow boosting of the output at 220 volt line to line voltage. Figs 4(a) and 4(b) illustrate that the proposed system and its control structure are capable of inverting and boosting the input DC voltage to the required ac level. The inverter output shows almost sinusoidal characteristics with a low harmonic distortion where the load voltage THD=3.33%. Also, the proposed control strategy ensures symmetrical load currents having a pure sine wave with very low harmonics (THD equal 0.87%) as shown in Fig. 4(c) and 4(d)

Technical Requirements for Connecting Small Scale PV (ssPV) [19]. The results comply with The IEEE 929, IEEE 1547 and IEC 61727-2004

standards that limit the (THD) of the current produced from the PV system to be < 5% and the individual harmonic components for each harmonic from 3rd to 9th to <4%. Oher

Components should not exceeds 2%.[19]. It may be emphasised that the THD spectrum id detailed up to

the 20th as the higher components are found not significant.

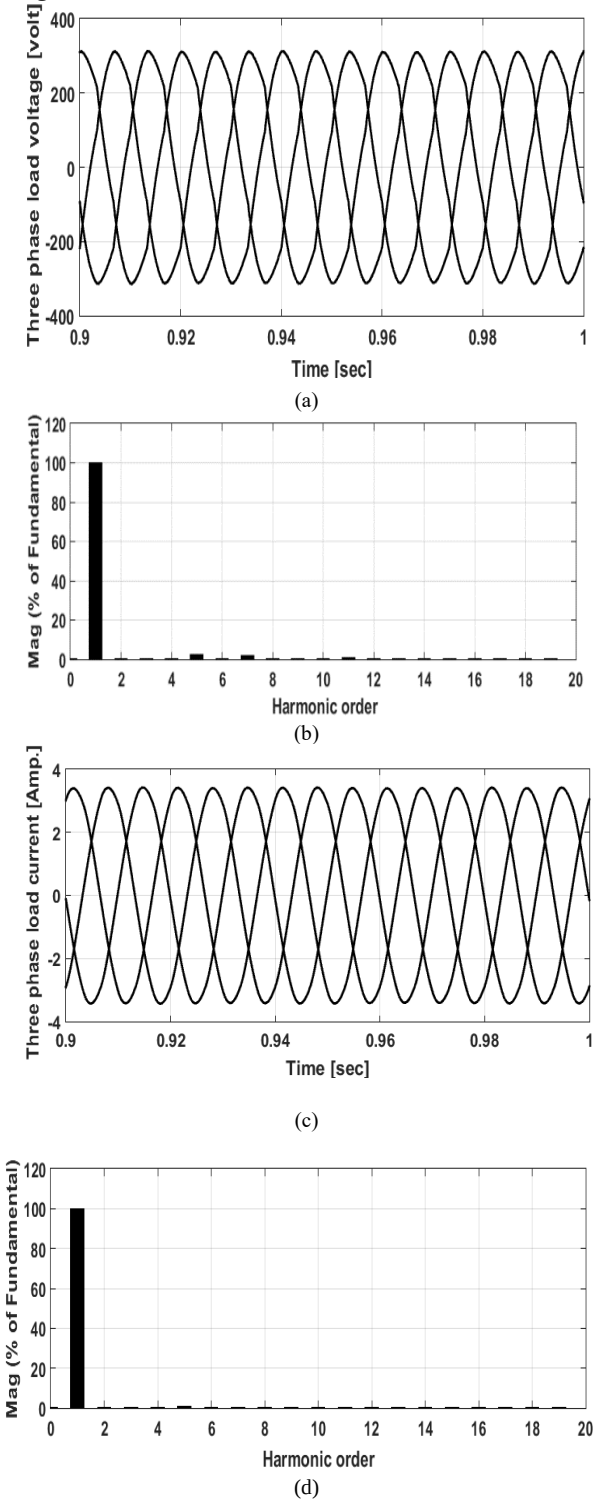


Fig. 4. The steady state results of the proposed inverter; (a) Three phase load voltages; (b) Harmonics spectrum of load voltage; (c) Three phase load currents; and (d) Harmonics spectrum of load current.

The proposed system is subjected to a step change in the reference voltage from 220V to 270V for a duration of 0.4 sec and the results are shown in Fig. 5. In Fig. 5(a), it could be shown that the output load voltage and its change during reference voltage change (proportional relationship), Also from the figure, a maintained sinusoidal waveform of the load voltage could be achieved with fast dynamic response; Fig. 5(b) shows the load current waveform and its variation with the reference voltage change as its increase as reference voltage increase. The results shown in Fig. 5(c) illustrate clearly that the new topology and control structure enabled the system to follow the reference value precisely.

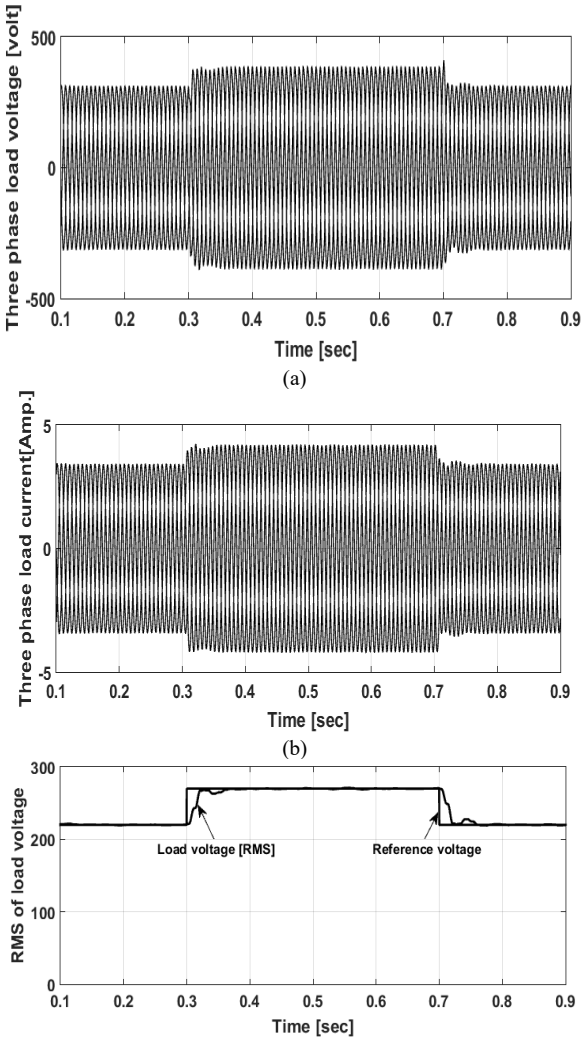
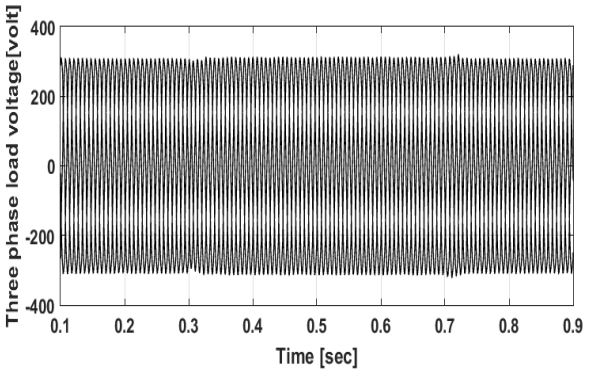


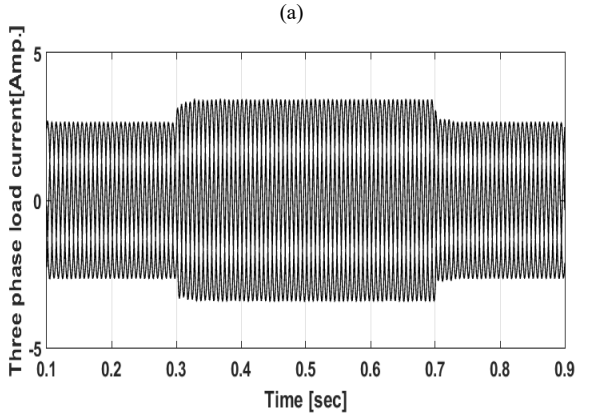
Fig. 5. The transient state results of the proposed circuit at step change in reference voltage; (a) Load voltage; (b) Load current; (c) RMS of load voltage.

The output current and voltage response to a 30% increase in the load is given in Fig. 6. The result shown in Fig. 6(a) shows that the load voltage has a constant amplitude sine wave even if there is a

sudden change. Fig. 6(b) shows a fast response sinusoidal waveform for the output current. The results also demonstrate good voltage regulation as might be observed from Fig. 6(c).



(a)



(b)

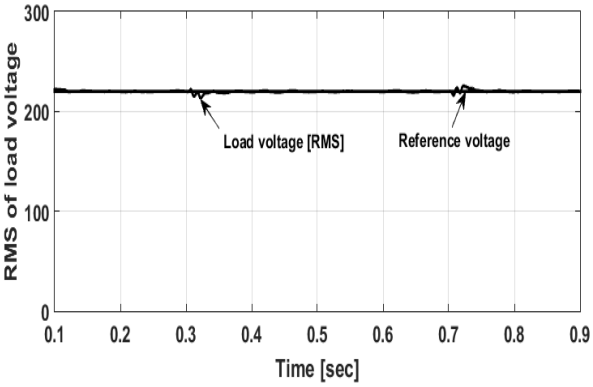
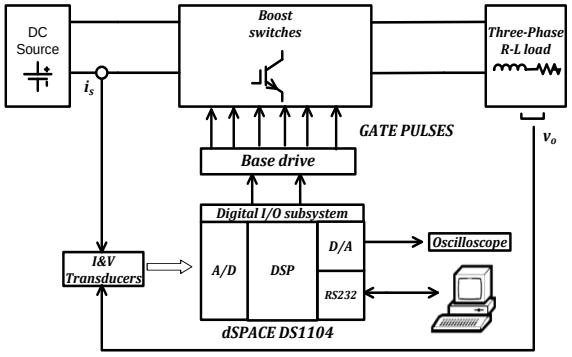


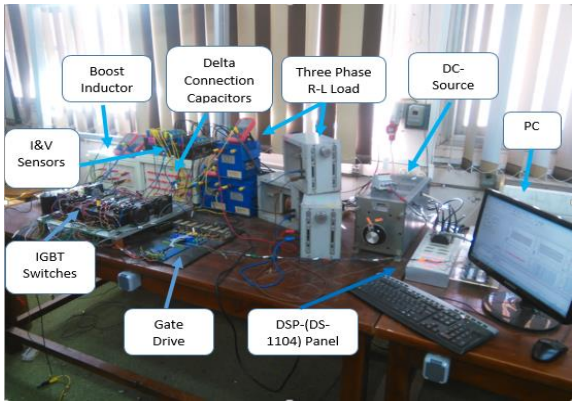
Fig. 6. The transient state results of the proposed inverter at 30% increase in load; (a) Three phase load voltages; (b) Three phase load currents; and (c) RMS of load voltage.

5. Experimental Results

To evaluate the performance of the proposed inverter with the proposed control, a laboratory prototype is built using a digital signal processor board (DS1104). The block diagram of the experimental setup and real view of the complete control system are shown in Figs. 7(a) and 7(b), respectively. The system parameters are reported as before in Appendix



(a)



(b)

Fig. 7 Block diagram of the Experimental setup of the proposed circuit.

Figure 8 shows the steady-state experimental results of the proposed circuit using the new control strategy. The DC supply voltage is kept constant at 25 volt and the reference voltage is controlled to allow boosting of the output at a reference voltage of 50 volt line to line voltage. Fig. 8(a) illustrates that the new topology and its control structure are capable of boosting the input dc voltage to the required ac level with almost sinusoidal characteristics with the THD spectrum shown Fig. 8(b). Also, the three phase load currents are nearly sinusoidal waveform, Figs. 8(c), with THD equal to 3.36%, Fig. 8(d).

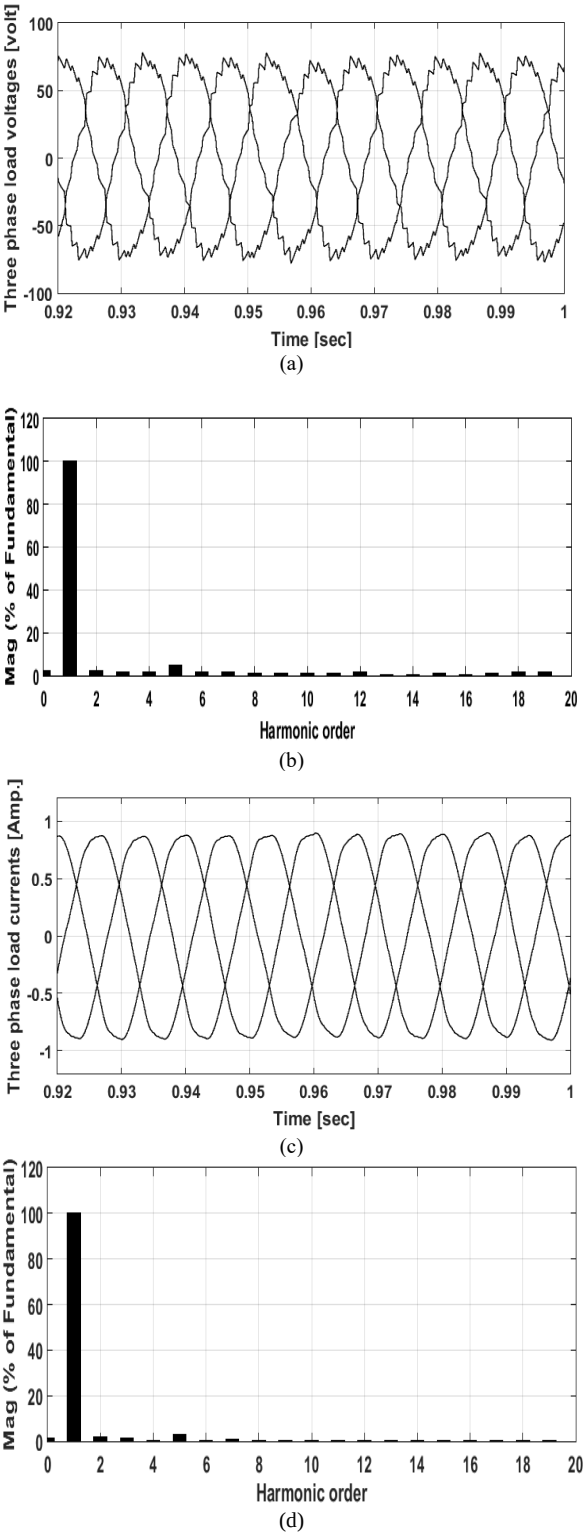


Fig. 8. The steady state experimental results of the proposed inverter; (a) Three phase load voltages; (b) Harmonics spectrum of load voltage; (c) Three phase load currents; and (d) Harmonics spectrum of load current.

The experimental results of output load voltages, output load currents, and RMS value of load voltage due to a step change in reference voltage from 50 to 70 volt for a duration of 0.4 sec are shown in Fig. 9, respectively. The results show that the proposed control strategy has a high control ability to drive the circuit to the new reference values which ensures the system capability

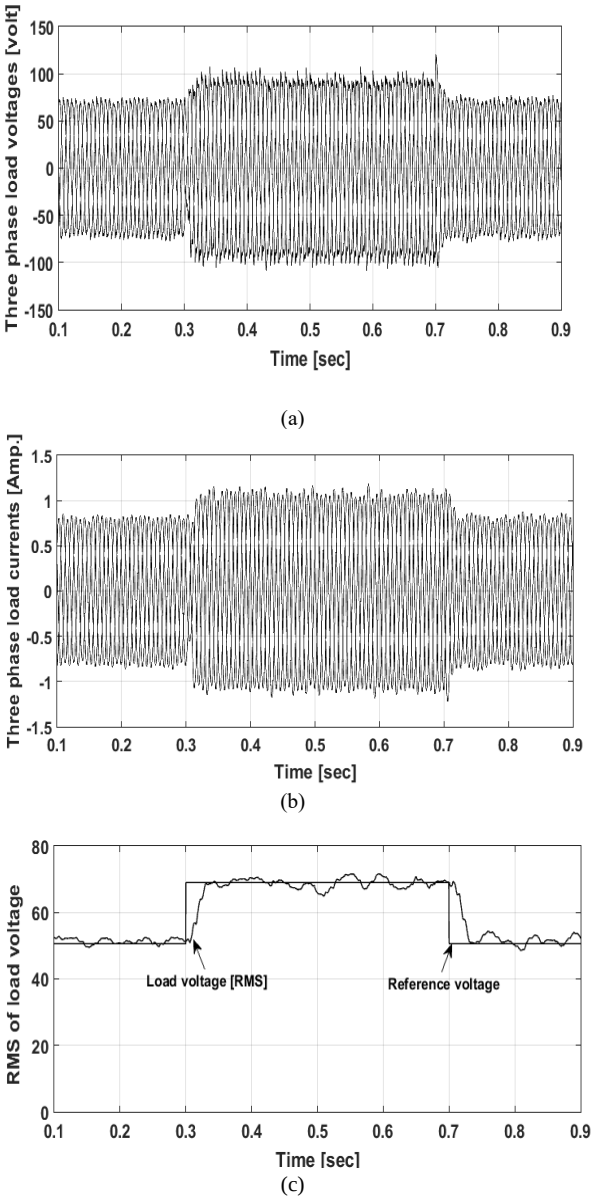


Fig. 9. The experimental results of the proposed inverter at step change in reference voltage; (a) Three phase load voltages; (b) Three phase load currents; and (c) RMS of load voltage.

Also the three phase output load voltages, currents and voltage response to a 30% increase in the load are investigated experimentally as given in Fig. 10. This results shows that the topology proposed with its

control methodology has a high response back to the reference value during the load change, which ensures the efficiency of the overall circuit topology proposed.

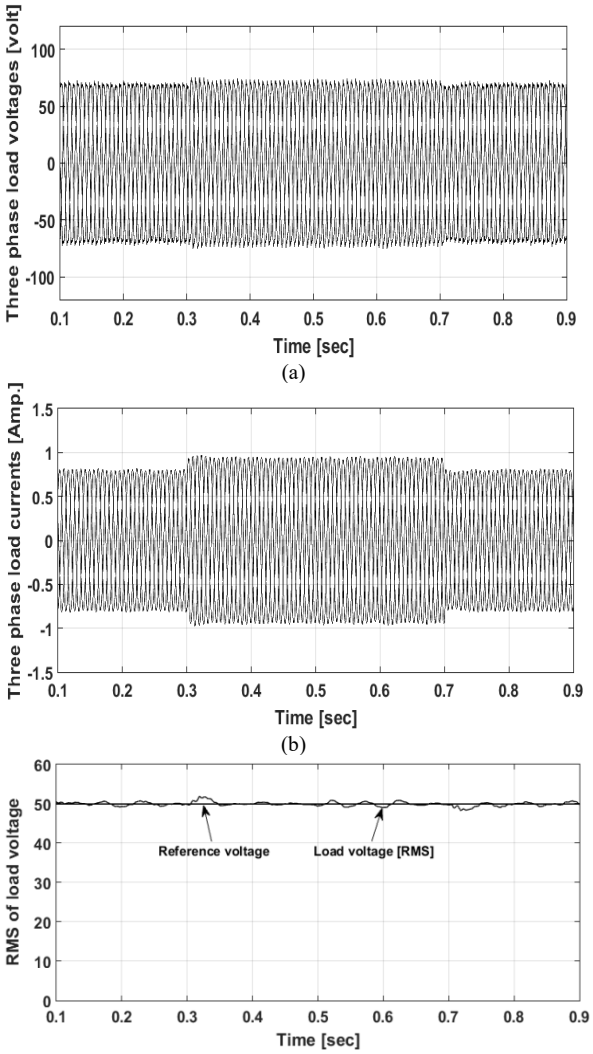


Fig. 10. The experimental results of the proposed inverter at 30% increase in load; (a) Three phase load voltages; (b) Three phase load currents; and (c) RMS of load voltage.

Finally the proposed inverter is tested experimentally using 200 watt PV panels. Figs. 11(a) and 11(c) show that the proposed topology with its proposed control structure is capable of boosting and inverting the input DC voltage from the PV source to AC level with almost sinusoidal characteristics. This is confirmed by Figs. 11(b) and 11(d) that indicate the THD complies with its standard, which ensures the reliability of the proposed boost inverter.

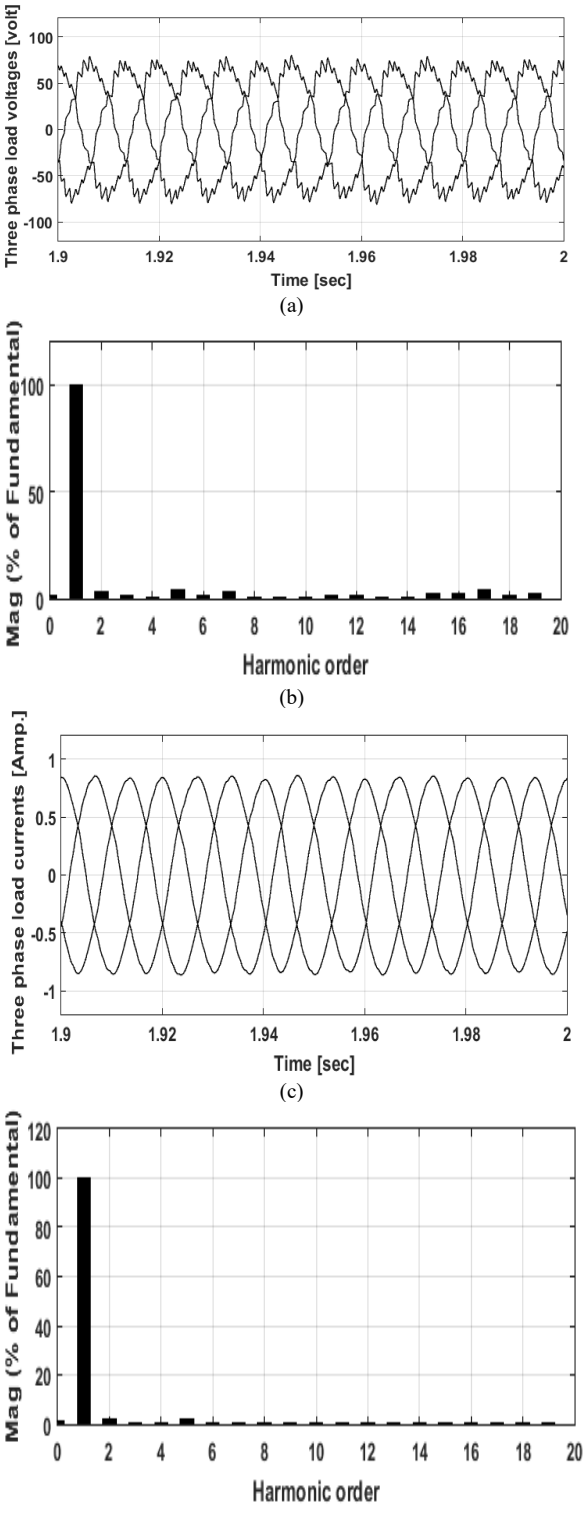


Fig. 11. The experimental results of the proposed inverter when supplied from PV source; (a) Three phase load voltages; (b) Harmonics spectrum of load voltage; (c) Three phase load currents; and (d) Harmonics spectrum of load current.

6. Conclusion

The paper presented a single-stage three-phase boost inverter with a new control strategy. The proposed control strategy provide a well-regulated sinusoidal AC output with low harmonic distortion levels. The proposed inverter is tested theoretically by computer simulation when subjected to a variety of disturbances. The simulation results are verified experimentally using the DSP-based laboratory model. A good agreement between theoretical and experimental results with nearly a sinusoidal wave forms was shown. The THD measurements were conducted over the experiment time and the results are obtained from the digital DSP output signal using the FTT analysis. In addition, the proposed single-stage three-phase boost inverter offers a good voltage regulation of the synthesized output voltage and current waveforms when system is subjected to sudden changes in loads.

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Appendix A

Data parameters of the Three-phase proposed inverter:

L_s =30 mH,

R_s =1Ω,

$C_{ab} = C_{bc} = C_{ca}$ = 70 µF,

$R_{aL} = R_{bL} = R_{cL}$ = 35 Ω,

$L_{aL} = L_{bL} = L_{cL}$ = 125 mH.