A NOVEL 4-NEURON HOPFIELD ANN USING SET TECHNOLOGY

دائرة جديدة لشبكة هوبفيلد العصبونية ذات الأربع خلايا
باستخدام تكنولوجيا إختراق الإلكترون الواحد (النانومترية)

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الخلاصة:

إن تكنولوجيا إختراق الإلكترون الواحد (النانومترية) تقدم إمكانية أكبر لتصغيرأبعاد المكونات الإلكترونية الحديثة مقارنة بالإمكانيات المتوقعة لتكنولوجيات السيليكون المعروفة (مثل تكنولوجيا معدن-أكسيد-شبه موصل المزدوجة). إن تكنولوجيا إختراق الإلكترون الواحد تعطى القدرة على التحكم فى حركة الإلكترونيات فى الدوائر المصممة. فى هذا البحث سنقوم بإستعراض بعض دوائر الإلكترون الواحد الأساسية فى الأبحاث المنشورة حديثا، وسيتضمن ذلك تفاصيل هذه الدوائر بما فيها قيم المكونات المستخدمة والنتائج المتوقعة لإستخدام هذه الدوائر بإستخدام برنامج المحاكاه على الكمبيوتر (سيمون 2). وفى نهاية البحث سنقدم التصميم الكامل لدائرة إلكترون واحد جديدة تنفذ شبكة هوبفيلد العصبونية المكونة من أربع خلايا مع نتائج المحاكاه على الكمبيوتر.

Abstract:

Single Electron Tunneling (SET) technology introduces more potential for feature size reduction compared with well-established silicon-based CMOS technology. The SET technology offers the ability to control the motion of individual electrons in the designed circuits. In this paper, some of the basic Single Electron Circuits (SECs), found in the literature, are reviewed. The complete schematic diagrams of these basic SECs (inc. parameters for used devices) along with the corresponding simulation results (using the famous Monte Carlo simulator; SIMON 2.0) of these SEC are included. Finally, a novel 4-neuron Hopfield ANN SEC is introduced. The full design (inc. detailed schematic diagram) and its SIMON 2 simulation results are included.

1. Introduction:

The Single Electron Tunneling (SET) technology is the most promising future technology generations to meet the required increase in density and performance and decrease in power dissipation [1-2]. The main device of the SET circuits is the tunnel junction through which individual electrons can move in a controlled manner [3].

A decade ago, the basic physics of SET was well understood and designing useful Single Electron Circuits (SEC) became the important research area [4-5]. In the past few years, some basic building blocks for SEC had been introduced in the literature [6-9].

In this paper, we first briefly discuss the basic physics of SET in section 2. We review some of the SEC basic building blocks that were introduced in the literature, in Section 3. The full design (inc. detailed schematic diagrams with all parameters for used devices) and simulation results (using the famous Monte Carlo simulator; SIMON 2 [10]) are included. In Section 4, a novel 4-neuron Hopfield Artificial Neural Network (ANN) SEC is introduced. The full design and SIMON 2.0 simulation results of the developed Hopfield ANN SEC are presented. The conclusions are provided in Section 5 followed by the used references in Section 6.

2. The Basic Physics of SET:

The main component of SEC is the tunnel junction that can be implemented using silicon or metal-insulator-metal structures, GaAs quantum dots, etc.

The tunnel junction can be thought of as a leaky capacitor [11]. For very small tunnel junctions (hence, very small capacitance C_j), the movement of only one electron, from one side of the tunnel junction to the other, may produce a noticeable change e/C of the voltage across the tunnel junction. Note that the above $C = C_j + C_e$ where C_e is the equivalent capacitance of the remainder of the circuit, as viewed from the tunnel junction's perspective.

The discreteness of the electrical charge e leads to the Coulomb blockade effect that is widely known in the field of single-electronics. The critical voltage V_c (the voltage needed in order to make one electron tunnel through the junction) is given by [6]:

$$V_c = e/2C \qquad (1)$$

The Coulomb blockade effect is the suppression of electron tunneling across the tunnel junction at voltages $|V| < e/2C$. This means that for such voltages, there will be no increase in the electrostatic energy of the junction capacitor: $CV^2/2$ (in the case of such increase, the energy would be [4]: $C(V \pm e/C)^2/2$.

Today's well-established technologies uses metal junctions with an area about 50×50 nm^2 that lead to a typical capacitance and its corresponding voltage scale (e/C) in the order of 100 aF and 1 mV, respectively.

To avoid the effects of thermal fluctuations on SEC, the thermal energy $k_B T$ should be much less than the typical one-electron charging energy ($eV = e^2/2C$) [4],

$$k_B T << e^2/2C \qquad (2)$$

The above condition limits the practical use of SEC since the working temp. is restricted to be < 1 K. For a room operating temperature (300 K), junction capacitances should decrease to the range of 0.1 aF. To reach this low capacitance level, the size of the devices should go below few nanometers and single electronics enters the areas of atomic physics and chemistry [4].

3. The Basic SEC Building Blocks:

Some of the basic SEC building blocks, found in the literature, are reviewed in this section. The full design (inc. detailed SEC) and SIMON 2 simulation results are also included.

3.1 The Single Electron Box:

The Single Electron Box (SEB) is the simplest device using SET effect. The SEB is composed of one capacitor and one tunnel junction [8].

Fig. 1 shows one possible way of constructing the SEB along with the sawtooth-like output characteristics using SIMON 2. In this configuration of the SEB: with the linear increase of VIN, VOUT increases until it reaches the critical value of $e/2(C_j+C_o)$. Then the tunneling occurs and as a result, the charge goes down and VOUT decreases instantaneously to become $-e/2(C_j+C_o)$. The above process repeats giving rise to the sawtooth-like output.

Fig. 2 shows the other possible way of constructing the SEB along with its output. In this configuration, VOUT increases linearly until the tunneling occurs, then there will be a sudden increase in VOUT due to the charge transfer. The above process repeats giving rise to the linear-step-like output.

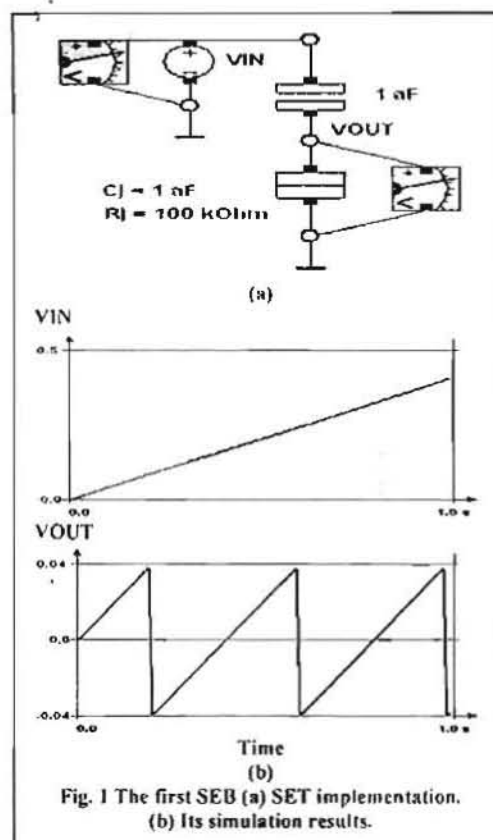

Fig. 1 The first SEB (a) SET implementation.
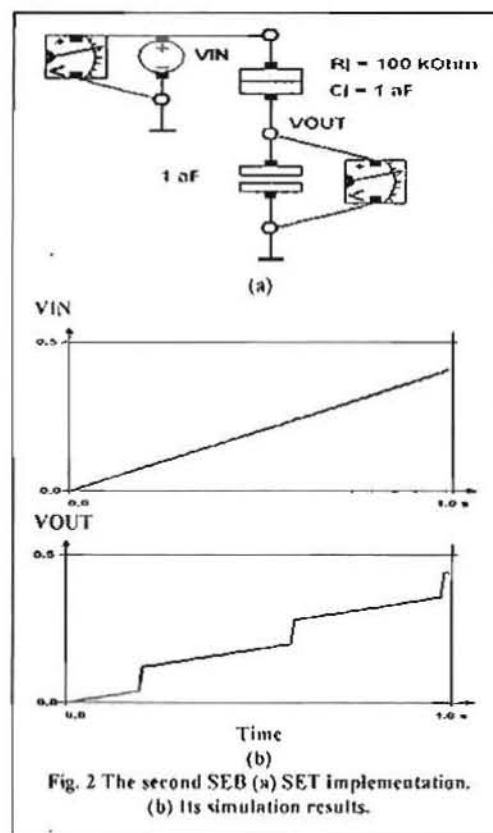(b) Its simulation results.

Fig. 2 The second SEB (a) SET implementation.
(b) Its simulation results.

3.2 The Linear Threshold Gate:

The general Linear Threshold Gate (LTG) shown in Fig. 3 is able to compute any linearly separable Boolean function represented by:

$$Y = sgn\{F(X)\} = \begin{cases} 0 \text{ if } F(X) < 0 \\ 1 \text{ if } F(X) \geq 0 \end{cases} \quad (3)$$

$$F(X) = \sum_{i=1}^{n} \omega_i x_i - \psi \quad (4)$$

Where x_i are the n Boolean inputs and ω_i are the corresponding n integer weights.

The LTG compares between the weighted sum of inputs and the threshold value ψ to determine if the output is logic 1 or logic 0 [7].

Note that this LTG SEC is capable of implementing both positive and negative weights. This can be accomplished by connecting the corresponding inputs (through appropriate capacitors) to nodes POS and NEG (see Fig. 3), respectively.

Note also that the threshold value ψ is implemented and can be adjusted by the capacitor C_b and the external voltage V_b.

Due to the passive nature of the LTG circuit, an added buffer/inverter circuit at its output is essential for the correct operation of the LTG circuit. To get both the normal and inverted output, one can add two cascaded inverters at the LTG output [7].

4. The Hopfield ANN SEC:

The Hopfield ANN is a fully connected single-layer auto-associative network. The connections in a Hopfield ANN typically have the following restrictions:
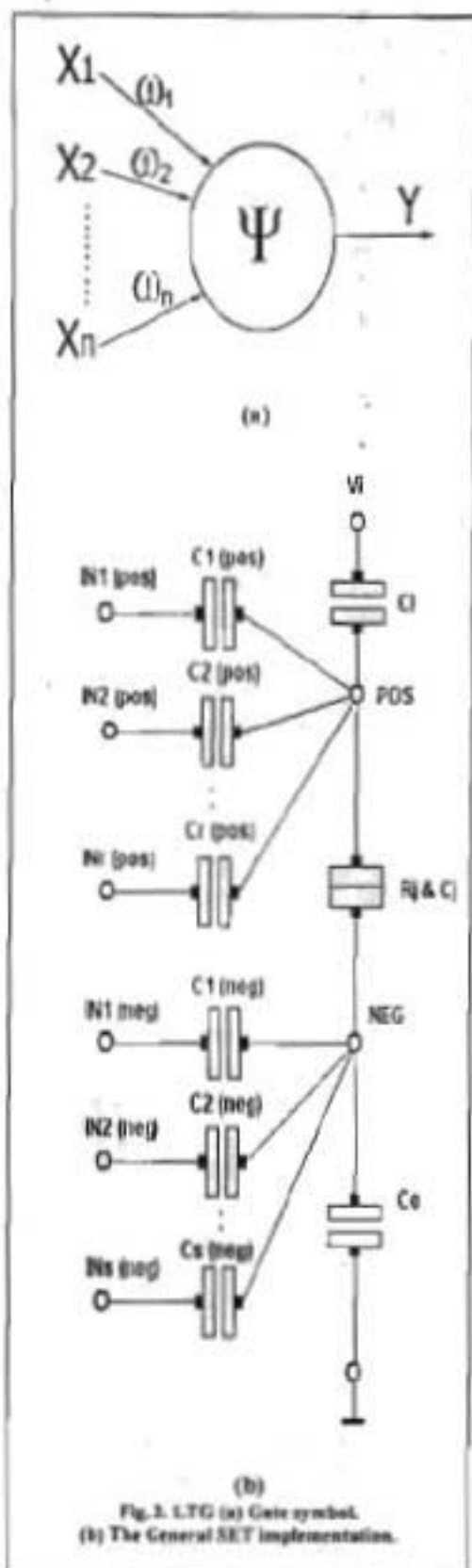

(a)

(b)

Fig. 3. LTG (a) Gate symbol.
(b) The General SET implementation.

1. Each neuron is connected to every other neuron (except itself).

$$w_{ii} = 0, \forall i$$

2. The Hopfield ANN is guaranteed to converge to a stable state due to the symmetric nature of its connections [11].

$$w_{ij} = w_{ji} \forall i, j$$

Hopfield nets can have binary threshold units that take on either values of 1 or -1, or values of 1 or 0. So, the two possible definitions for unit i's activation, a_i, are:

$$a_i \leftarrow \begin{cases} 1 & \text{if } \sum_j w_{ij}s_j > \theta_i, \\ -1 & \text{otherwise.} \end{cases} \quad (5)$$

$$a_i \leftarrow \begin{cases} 1 & \text{if } \sum_j w_{ij}s_j > \theta_i, \\ 0 & \text{otherwise.} \end{cases} \quad (6)$$

Where:

w_{ij} is the strength of the connection weight from unit j to unit i (the weight of the connection).

s_j is the state of unit j.

θ_i is the threshold of unit i.

Hopfield ANNs can perform robust content-addressable memory systems. For example, if we train a Hopfield net with four units so that the state 1001 is an energy minimum, and we give the network the state 1000 it will converge to 1001. When a Hopfield ANN is trained to recognize a binary pattern, it also recognizes the inverse of that bit pattern. As a result, the above Hopfield ANN would also recognize 0110 [11].

Because each neuron can potentially be connected to every other neuron, a two-dimensional array can be used to show the weight matrix. For example, the values shown in Table 1 show the

correct values to use to recall the pattern 1001.

Table 1: Weights used to recall 1001

Neurons	1	2	3	4
1	0	-1	-1	1
2	-1	0	1	-1
3	-1	1	0	-1
4	1	-1	-1	0

When a Hopfield ANN is trained to recognize a binary pattern, it also recognizes the inverse of that bit pattern. As a result, the above connection weight matrix would also recognize 0110 [11].

The developed SET ANN neuron is shown in Fig. 4. It consists of the SET LTG introduced in [6] followed by a SET buffer/inverter introduced in [9]. Note that in this design, the buffer/inverter is connected to the POS node rather than the NEG node. This leads to non-inverting output that will make designing SET ANN circuits simpler.

The synapses of the ANN are implemented as capacitors that can be connected to either the POS node or the NEG node depending on the sign of the associated weight.

A 4-neuron Hopfield ANN is trained to recognize the binary patterns 1001 and 0110 using the online Hopfield Neural Network Applet [12]. The binary weight matrix obtained from the above training is mapped to the SET design shown in Fig. 5.

The complete Hopfield ANN SEC is simulated using the famous Monte Carlo simulator SIMON 2 and the results are summarized in Table 2.
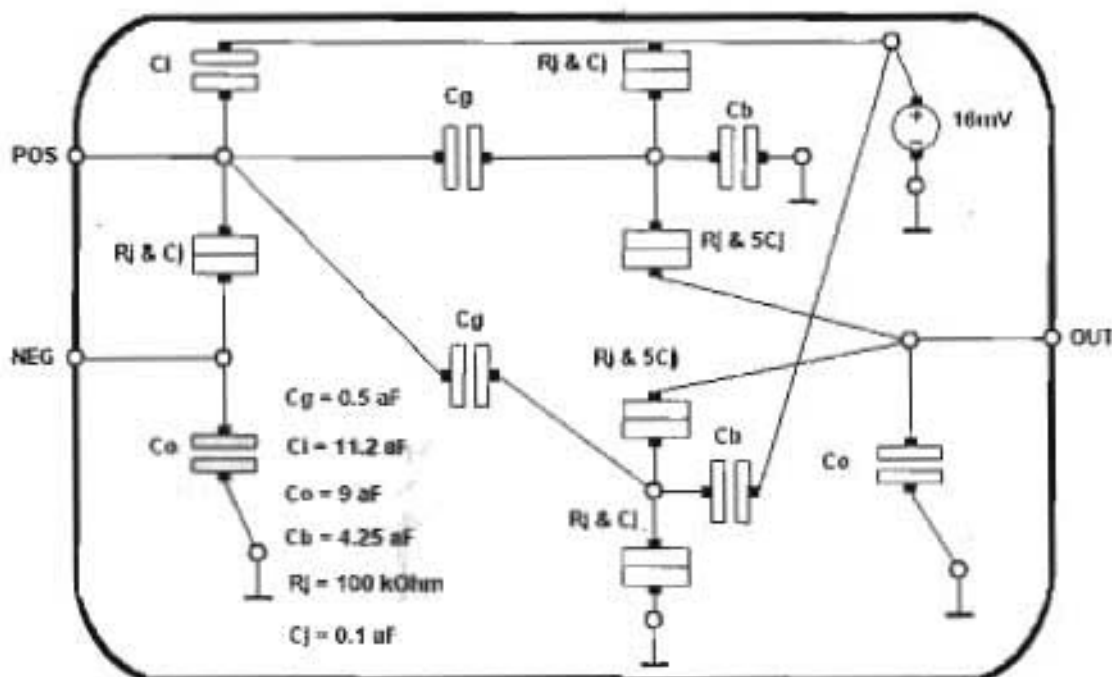
Fig. 4. The schematic diagram of the developed SET ANN neuron (inc. all parameters used in SIMON 2.0).

It is worth noting here that the simulation results show that the Hopfield ANN SEC is tolerant to an error in only one of the four binary bits of the input pattern.

5. Conclusions:

The developed SET ANN neuron is shown in Fig. 2. It consists of the SET LTG introduced in [6] followed by a SET buffer/inverter introduced in [12]. Note that in this design, the buffer/inverter is connected to the POS node rather than the NEG node. This leads to non-inverting output that will make designing SET ANN circuits simpler.

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6. References:

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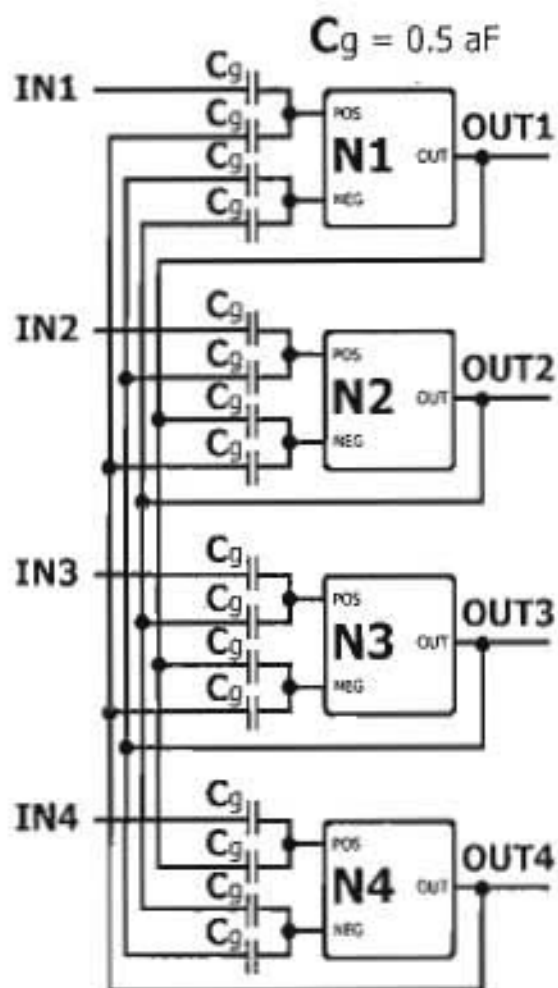[12] Jeff Heaton, (2006, Aug 10). http://www.heatonresearch.com [URL]: http://www.heatonresearch.com/articles/61/page1.html

Fig. 5. The developed 4-neuron Hopfield ANN.

TABLE 2
INPUT AND OUTPUT PATTERNS FOR
THE DEVELOPED 4-NEURON HOPFIELD ANN

Input Patterns	Output Patterns
1001	1001
0001	1001
1101	1001
1011	1001
1000	1001
0110	0110
1110	0110
0010	0110
0100	0110
0111	0110
0000	Don't Care
1111	Don't Care
0011	Don't Care
1100	Don't Care
0101	Don't Care
1010	Don't Care