Mansoura University
Faculty of Engineering
Communications and Electronics Engineering Department

| Digital Circuits 1-Term Exam | Exam Time: 3 hours |
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| Exam Date: June 12th, 2012 | Total Marks: 70 Marks |
| 1st year Electronics - 2nd Term |  |

Important Instructions:
1 This exam contains:

## pages $2 \& 3$

25 MCQs (4 choices each) --> Mark your answer selection in the MCQ answer sheet in the middle of the answer booklet Q1-Q25
(25 Marks)
Note: answer all questions.
each correct answer will be marked with (+1) mark.
each wrong or unanswered question will get a zero mark.

## page 4

3 Questions (technical questions) --> Write your answers in the booklet
(45 Marks)

2 No calculators are allowed in this exam.

My best wishes to YOU!
Dr. Sameh Rehan
Note: This exam has questions on both sides of the questions' sheets.

| Digital Circuits 1 - exam (3 hrs) | June 12th, 2012 |
| :--- | :--- |
| 1st year electronics engineering students | page 2 |

Answer the following 25 MCQs in the MCQ sheet in the answer booklet: (Total of 25 Marks) (+1 Mark for each correct answer, zero Mark for each wrong or unanswered question)

Q1 Compared to analog systems, digital systems
(1) are less prone to noise
(3) can handle much higher power
(2) can represent an infinite number of values
(4) all of the above

Q2 The number of values that can be assigned to a bit are
(1) one
(3) three
(2) two
(4) ten

Q3 The time measurement between the $50 \%$ point on the leading edge of a pulse to the $50 \%$ point on the trailing edge of the pulse is called the
(1) rise time
(3) period
(2) fall time
(4) pulse width

Q4 The time measurement between the $90 \%$ point on the trailing edge of a pulse to the $10 \%$ point on the trailing edge of the pulse is called the
(1) rise time
(3) period
(2) fall time
(4) pulse width

Q5 The reciprocal of the frequency of a clock signal is the
(1) rise time
(3) period
(2) fall time
(4) pulse width

Q6 If the period of a clock signal is 500 ps , the frequency is
(1) 20 MHz
(3) 2 GHz
(2) 200 MHz
(4) 20 GHz

Q7 AND, OR, and NOT gates can be used to form
(1) storage devices
(3) data selectors
(2) comparators
(4) all of the above

Q8 A shift register is an example of a
(1) storage device
(3) data selector
(2) comparator
(4) counter

Q9 A device that is used to switch one of several input lines to a single output line is called a
(1) comparator
(3) counter
(2) decoder
(4) multiplexer

Q10 For the binary number 1000 , the weight of the column with the 1 is
(1) 4
(3) 8
(2) 6
(4) 10

Q11 The 2's complement of 1000 is
(1) 0111
(3) 1001
(2) 1000
(4) 1010

Q12 The fractional binary number 0.11 has a decimal value of
(1) $1 / 4$
(3) $3 / 4$
(2) $1 / 2$
(4) none of the above

| Digital Circuits 1-exam (3 hrs) | June 12th, 2012 |
| :--- | :--- |
| 1st year electronics engineering students | page 3 |

Q13 The hexadecimal number 2 C has a decimal equivalent value of
(1) 14
(3) 64
(2) 44
(4) none of the above

Q14 When two positive signed numbers are added, the rêsult may be larger that the size of the original numbers, creating overflow. This condition is indicated by
(1) a change in the sign bit
(2) a carry out of the sign position

Q15 The number 1010 in BCD is
(1) equal to decimal eight
(3) equal to decimal twelve
(2) equal to decimal ten
(4) invalid

Q16 An example of an unweighted code is
(1) binary
(3) BCD
(2) decimal
(4) Gray code

Q17 An example of an alphanumeric code is
(1) hexadecimal
(3) BCD
(2) ASCII
(4) octal

Q18 A 2-input gate produces a HIGH output only when the inputs agree. This type of gate is a(n)
(1) NAND gate
(3) XNOR gate
(2) XOR gate
(4) NOR gate

Q19 A Boolean expression that is in standard SOP form is
(1) the minimum logic expression
(3) has every variable in the domain in every tern
(2) contains only one product term
(4) none of the above

Q20 Adjacent cells on a Karnaugh map differ from each other by
(1) one variable
(3) three variables
(2) two variables
(4) answer depends on the size of the map

Q21 The two types of gates which are called universal gates are
(1) $\mathrm{AND} / \mathrm{OR}$
(3) AND/NAND
(2) NAND/NOR
(4) OR/NOR

Q22 For a negative-logic pulse, the leading edge is the $\qquad$ .
(1) LOW-to-HIGH transition
(3) rising edge
(2) positive-going edge
(4) tfegative-going edge

Q23 The number of binary digits (bits) that are required to count to decimal 225 is:
(1) 8
(3) 6
(2) 7
(4) 5

Q24 In the 2-input $\qquad$ gate, a High input gives a Low output.
(1) NAND
(3) AND
(2) NOR
(4) OR

Q25 The $\qquad$ circuit converts a specific coded form into known information.
(1) demultiplexer
(3) decoder
(2) multiplexer
(4) encoder

| Digital Circuits 1 - exam (3 hrs) | June 12th, 2012 |
| :--- | ---: |
| 1 st year electronics engineering students | page 4 |

Answer the following 3 technical questions in the answer booklet: (total of 45 Marks) (both wrong answers and unanswered questions have zero marks)

Q1. For adder logic circuits: (total of 15 marks)
a- draw the logic symbol and the truth table of the half-adder logic circuit.
b- draw the logic symbol and the truth table of the full-adder logic circuit. (4 marks)
c- implement a half-adder using simple (AND, OR, NOT) logic gates.
d- form a full-adder logic circuit using half-adders and any required gates.

Q2. For the 7-segment decoding logic, a BCD number is used as the input and the 7 outputs are used to activate the corresponding segments of the display. The arrangement of segments is as shown:
(total of 25 marks)
a- write down the truth table (use $X$ to represent don't care output) for all seven segments $a, b, c, d, e, f$, and $g$.
b- develop the optimized sum-of-products Boolean logic expression of the "c" output segment using Karnaugh map.
c- develop the optimized product-of-sums Boolean logic expression of the " $g$ " output segment using Karnaugh map.
d- develop the optimized logic circuit using appropriate gates for the logic expressions developed in the previous two questions for
 output segments "c" and "g".
(6 marks)

Q3. If the data-select inputs to the shown multiplexer are sequenced as shown by the shown waveforms, determine the output for the following input states:
Do $=0, D 1=1, D 2=1, D 3=0$
(5 Marks)


