Mansoura University Faculty of Engineering Communications and Electronics Engineering Department

Digital Circuits 1 - Term Exam	Exam Time:	3 hours
Exam Date: June 12th, 2012	Total Marks:	70 Marks
1st year Electronics - 2nd Term		

Important Instructions:

1 This exam contains:

C

pages 2 & 3

25 MCQs (4 choices each) --> Mark your answer selection in the MCQ answer sheet in the middle of the answer booklet Q1-Q25

(25 Marks)

Note: answer all questions.

each correct answer will be marked with (+ 1) mark.

each wrong or unanswered question will get a zero mark.

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3 Questions (technical questions) --> Write your answers in the booklet

(45 Marks)

2 No calculators are allowed in this exam.

My best wishes to YOU!

Dr. Sameh Rehan

Note: This exam has questions on both sides of the questions' sheets.

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Answer the following 25 MCQs in the MCQ sheet in the answer booklet: (Total of 25 Marks) (+ 1 Mark for each correct answer, zero Mark for each wrong or unanswered question)

	Compared to analog systems, digital systems		ý					
1	are less prone to noise		an handle much higher power					
2	can represent an infinite number of values		ll of the above					
	The number of values that can be assigned to	a bit	are					
1	one	3 th	nree					
2	two	④ te	en					
Q3	The time measurement between the 50% point							
	to the 50% point on the trailing edge of the po	lse is	s called the					
1	rise time		eriod					
2	fall time	-	ulse width					
Q4	The time measurement between the 90% point on the trailing edge of a pulse							
	to the 10% point on the trailing edge of the pulse is called the							
\bigcirc	rise time	-	eriod					
2	fall time	@ p	ulse width					
	The reciprocal of the frequency of a clock sig							
1	rise time	-	eriod					
2	fall time	④ pi	ulse width					
Q6	If the period of a clock signal is 500 ps, the fr	equer	ncy is					
1	20 MHz		GHz					
2	200 MHz	④ 20	0 GHz					
Q7	AND, OR, and NOT gates can be used to form							
1	storage devices	3 da	ata selectors					
2	comparators	(4) al	ll of the above					
Q8	A shift register is an example of a							
1	storage device	3 da	ata selector					
2	comparator		ounter					
Q9	A device that is used to switch one of several input lines to a single output line is called a							
1	comparator	3 cc	ounter					
2	decoder	@ m	nultiplexer					
Q10	0 For the binary number 1000, the weight of the column with the 1 is							
1	4	38						
2	6	(4) 10	0					
Q11	The 2's complement of 1000 is							
1	0111	3 1						
2	1000	④ 10	010					
Q12	Q12 The fractional binary number 0.11 has a decimal value of							
1	1/4	3 ³ /4						
2	1/2	4 n	one of the above					

D	Digital Circuits 1 - exam (3 hrs)		June 12th, 2012		
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13 T	he hexadecimal number 2C has a decimal ec	•			
D 14		3	64		
9 44			none of the above		
14 W	When two positive signed numbers are added	, th	e result may be larger that the size of		
th	ne original numbers, creating overflow. This	con	ndition is indicated by		
) a	change in the sign bit	3	a zero result		
) a	carry out of the sign position	4	smoke		
15 T	he number 1010 in BCD is				
1) ec	qual to decimal eight	3	equal to decimal twelve		
2 ec	qual to decimal ten	4	invalid		
16 A	in example of an unweighted code is				
	inary	3	BCD		
2 de	ecimal	4	Gray code		
17 A	In example of an alphanumeric code is				
	exadecimal	3	BCD		
2 A	SCII	4	octal		
18 A	2-input gate produces a HIGH output only	wh	en the inputs agree. This type of gate is $a(n)$		
	IAND gate		XNOR gate		
	COR gate		NOR gate		
	Boolean expression that is in standard SOP		0		
	ne minimum logic expression		has every variable in the domain in every terr		
	ontains only one product term		none of the above		
	djacent cells on a Karnaugh map differ from				
	ne variable		three variables		
	vo variables		answer depends on the size of the map		
	the two types of gates which are called <i>univer</i>				
	ND/OR		AND/NAND		
	IAND/NOR		OR/NOR		
	or a negative-logic pulse, the leading edge is				
	OW-to-HIGH transition		rising edge		
	ositive-going edge		tfegative-going edge		
•	he number of binary digits (bits) that are req				
\mathbb{D} 8	the number of binary digits (bits) that are req	3			
27		4			
-					
	n the 2-input gate, a High input gives		AND		
			OR		
	he circuit converts a specific coded for				
			decoder		
m	ultiplexer	4	encoder		

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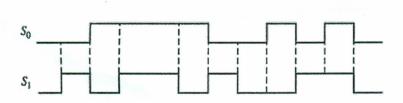
<u>Answer the following 3 technical questions in the answer booklet: (total of 45 Marks)</u> (both wrong answers and unanswered questions have zero marks)

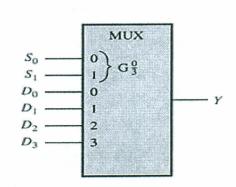
- Q1. For adder logic circuits: (total of 15 marks) a- draw the logic symbol and the truth table of the half-adder logic circuit. (4 marks)
 - b- draw the logic symbol and the truth table of the full-adder logic circuit.
 - c- implement a half-adder using simple (AND, OR, NOT) logic gates.
 - d- form a full-adder logic circuit using half-adders and any required gates.
- Q2. For the 7-segment decoding logic, a BCD number is used as the input and the 7 outputs are used to activate the corresponding segments of the display. The arrangement of segments is as shown:
 - a- write down the truth table (use X to represent don't care output) for all seven segments a, b, c, d, e, f, and g.
 (7 marks)
 - b- develop the optimized sum-of-products Boolean logic expression of the "c" output segment using Karnaugh map. (6 marks)
 - c- develop the optimized product-of-sums Boolean logic expression of the "g" output segment using Karnaugh map. (6 marks)
 - d- develop the optimized logic circuit using appropriate gates for the logic expressions developed in the previous two questions for output segments "c" and "g".
 - (6 marks)

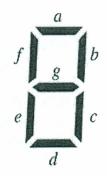
(total of 25 marks)

Q3. If the data-select inputs to the shown multiplexer are sequenced as shown by the shown waveforms, determine the output for the following input states: Do = 0, D1 = 1, D2 = 1, D3 = 0

(5 Marks)







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(4 marks)

(3 marks)

(4 marks)