University	:	*Menoufia*		*Date*	: *12/1/2020*
Faculty	:	*Electronic Engineering*		*Time*	: *3 Hours*
Department	:	Computer Science and Eng.		*No. of pages*	: *2*
Academic level	:	*3th Year*		*Full Mark*	: *70 Marks*
Course Name	:	Computer architecture		*Exam*	: *Final exame*
Course Code	:	CSE 361		*Examiner*	: *Dr. Mervat Mousa*

Answer all the following questions

Question NO 1 (8 marks)

a)Define (3 marks)

1)Data path **2) BUS and Data bus**

b)Draw and describe Von Neumann Architecture

Question NO 2 (9 marks)

a)Draw and explain the Static Random Access Memory (SRAM) and how to write operation 1 and 0

b)Why computer architecture changed in the last year ?

Question NO 3 (13 marks)

a) complete the words in the following sentence

1) The decoded instruction is stored in ----------

2) ALU adds the -------- and the --------- to form the effective address.

3) ---------- is used by virtually all modern microprocessors to enhance performance by overlapping the execution of instructions.

4)The functions of execution and sequencing are performed by using ----------

5) Any electronic holding place where data can be stored and retrieved later whenever required is --

b)Implement the following Boolean expression with the help of programmable logic array (PLA) and (PAL)

$$X=AB+AC'$$

$$Y = AB' +BC + AC'$$

Question NO 4 (18 marks)

A) For a direct-mapped cache design with a 32-bit address and byte-addressable memory, the following bits of the address are used to access the cache:

Tag	No of lines	Offset
31-10	9-5	4-0

1-What is the cache line size)?

2- Total cache size ?

3- Total memory size ?

4- in which line can map block No 137 ?

b) Draw the 2-way set associative cache memory after calculate the requirement from cache in problem A)

c) What is meant by write miss ? explain the two type of it using example Mem[1101110]=21543 with tage 1101

Question NO 5 (7 marks)

a) In a processor implementation, a data hazard can slow down the pipeline.
What is a data hazard? Give a short example using MIPS code that illustrates the problem and give a brief explanation of what the problem is.

b) Translate this C-style code into 4 lines of MIPS assembly code
Int t1=10,
int t2=3;
int t3=t1+2*t2

Question NO 6 (15 marks)

a) Drw the microarchitecture of load/ store and explain with example each MIPs instruction and type address of each

b) Give the setting for the control signals for the single cycle datapath shown on the next page when executing a sw instruction.

Control Signal	Setting		Control Signal	Setting
RegDst			ALUOp1	
Jump			ALUOp0	
Branch			MemWrite	
MemRead			ALUSrc	
MemtoReg			RegWrite	

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