Mansoura University		**Second Semester - Final Exam.**
Faculty of Engineering		**Exam Time: 3 Hours**
Department of Electronics and Communications Engineering		**Subject: Microprocessors**
		Course code: COM 9323
3rd Year Electronics & Comm.		**Exam Date: 11-6-2013**

Attempt all questions. Assume any missed data. Full Mark is 100

Q.1) Correct the errors, if any, in the following statements: **[15 Marks]**

a. Memory interface registers are used for holding intermediate results while processing instructions.
b. The size of each bus has no effect on the maximum size of memory that can be addressed.
c. In RISC, the CPU uses microcode to execute very comprehensive instruction set.
d. The AGP promises to replace the ISA bus in the most advanced system.
e. In register addressing, the Code segment register may not be the destination register.
f. Immediate data are variable data, while the data transferred from a register are constant data.
g. Scaled index addressing is unique to the 80386-P4 microprocessors.
h. The stack memory is FIFO (First-in, First-out) memory.
i. A dirty bit could be added to indicate whether the page has been changed.
j. Segmentation suffers from internal fragmentation.
k. The maximum mode was dropped beginning with the 80386 family.
l. The 80186/80188 are called embedded controllers.
m. The burst cycle in Pentium transfers four 32-bit numbers in 5 clocking periods.
n. The BIST is accessed on power up by placing a logic 1 on INIT while the RESET pin changes from 0 to 1.
o. The Pentium II is packaged on a Printed Circuit Board (PCB) instead of the integrated circuits of the past Intel microprocessors.

Q.2) Complete the following statements: **[10 Marks]**

a. To execute a program stored in main memory, the CPU controller performs .....
b. All commercial computers are based on..... concept, with programs and data sharing the same main memory.
c. ..... supports 8, 16, and 32-bit transfers between the personal computer and memory or I/O at rates of 8 MHz.
d. Memory can be accessed using any of three memory models; ....., ..., or .....
e. The ..... register contains the offset in the current code segment for the next instruction to be executed.
f. ..... applies to a MOV between a memory location and AL, AX, or EAX.
g. Program memory addressing modes used with the JMP instruction consist of three forms; ....., ..., and .....
h. Erasing an ..... requires a special tool that emits ultraviolet light.

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i. ..... is the time required to access the requested information in a given level of memory.

j. In ..... locality, accesses tend to be clustered in the address space.

k. ..... updates both the cache and the main memory simultaneously on every write.

l. ..... is an imaginary memory location in which all addressing issues are handled by the operating system.

m. The fully buffered 8088 requires ....., ..., and .....

n. In 80186, the interrupt controller operates in two modes; ..... or .....

o. ..... is a special way of handling memory accesses so the memory has additional time to access data.

p. The ..... defines information about the system's tables, tasks, and gates.

Q.3) Choose the most suitable answer in each of the following: **[5 Marks]**

1. The ..... pin is used to enable the most significant data bus bits in 8086 processor.
   a) AD0→AD7
   b) CLK
   c) BHE/S7
   d) ALE

2. In 80188, the ..... pin selects memory on the upper portion of the memory map.
   a) MCS0
   b) LCS
   c) MCS1
   d) UCS

3. The ..... pin is driven by a clock signal that is twice the operating frequency of the 80386.
   a) CLK
   b) BCLK
   c) PICCLK
   d) CLK2

4. In 80486, the ..... pin causes the µp to place its buses at high impedance state.
   a) BOFF
   b) BS8
   c) BRDY
   d) BREQ

5. In 80486, the ..... pin indicates that the coprocessor has detected an error condition
   a) IGNNE
   b) IERR
   c) FERR
   d) FRCERR

6. In Pentium, the ..... pin provides even parity for the memory address.
   a) APCHK
   b) AP
   c) BUSCHK
   d) PCHK

7. In Pentium, the ..... pin causes the µp to enter the system management mode of operation.
   a) SMM
   b) SMIACT
   c) SMI
   d) SMMEM

8. The ..... is an input that is placed at a logic 1 when the power supply and clock have stabilized in Pentium II.
   a) TESTHI
   b) POWERGOOD
   c) THERMTRIP
   d) WB/WT

9. The ..... pin must be connected to +2.5V through a 1K-10K resistor for proper Pentium II operation.
   a) TCK
   b) TESTHI
   c) TDI
   d) TDO

10. The ..... pin must be grounded to prevent Pentium from generating or receiving noise.
    a) SMI
    b) TDI
    c) EMI
    d) TDO
